WHAT IS CLAIMED:

1. An method for controlling a high-frequency switching module comprising a diplexer comprising first and second filter circuits F1, F2 for dividing signals received by an antenna to a receiving signal of a first transmitting/receiving system and a receiving signal of second and third transmitting/receiving systems, a first switching circuit SW1 disposed downstream of said first filter circuit F1 for switching a transmitting circuit TX1 and a receiving circuit RX1 of said first transmitting/receiving system by voltage applied from a control circuit VC1, and a second switching circuit SW2 disposed downstream of said second filter circuit F2 for switching a transmitting circuit TX2 of said second and third transmitting/receiving systems, a receiving circuit RX2 of said second transmitting/receiving system and a receiving circuit RX3 of said third transmitting/receiving system by voltage applied from control circuits VC2, VC3; said method comprising applying a positive voltage from said control circuit VC1 to said first switching circuit SW1 to connect the transmitting circuit TX1 of said first transmitting/receiving system to said antenna, and applying a positive voltage from said control circuit VC3.

2. A high-frequency switching module comprising a diplexer comprising first and second filter circuits F1, F2 for dividing signals received by an antenna to a receiving signal of a first transmitting/receiving system and a receiving signal of second and third transmitting/receiving systems, a first switching circuit SW1 disposed downstream of said first filter circuit F1 for switching a transmitting circuit TX1 and a receiving circuit RX1 of said first transmitting/receiving system by voltage applied from a control circuit VC1, and a second switching circuit SW2 disposed downstream of said second filter circuit F2 for switching a transmitting circuit TX2 of said second and third transmitting/receiving systems, a receiving circuit RX2 of said second

transmitting/receiving system and a receiving circuit RX3 of said third transmitting/receiving system by voltage applied from control circuits VC2, VC3;

said first switching circuit SW1 comprising an input/output terminal IP1 for inputting a receiving signal of said first transmitting/receiving system and outputting a transmitting signal, a connecting terminal P13 for inputting a transmitting signal from the transmitting circuit TX1 of said first transmitting/receiving system, a connecting terminal P16 for outputting a receiving signal of the first transmitting/receiving system to a receiving circuit RX1, a first diode DG1 disposed between said input/output terminal IP1 and said connecting terminal P13, a first inductance element LG1 disposed between said connecting terminal P13 and a ground, a second inductance element LG2 disposed between said input/output terminal IP1 and said connecting terminal P16, and a second diode DG2 disposed between said connecting terminal P16 and the ground;

said second switching circuit SW2 comprising an input/output terminal IP2 for inputting a receiving signal of said second and third transmitting/receiving systems and outputting a transmitting signal, a connecting terminal P7 for inputting a transmitting signal from a transmitting circuit TX2 of the second and third transmitting/receiving systems, an output terminal IP3 for outputting a receiving signal of the second and third transmitting/receiving systems, a connecting terminal P9 for outputting a receiving signal of the second transmitting/receiving system to a receiving circuit RX2, a connecting terminal P10 for outputting a receiving signal of said third transmitting/receiving system to a receiving circuit RX3, a third diode DP1 disposed between said input/output terminal IP2 and said connecting terminal P7, a third inductance element LP1 disposed between said connecting terminal P7 and the ground, a fourth inductance element LP2

disposed between said input/output terminal IP2 and said output terminal IP3, a fourth diode DP2 disposed between said output terminal IP3 and the ground, a fifth inductance element LD1 disposed between said output terminal IP3 and said connecting terminal P9, a fifth diode DD1 disposed between said connecting terminal P9 and the ground, a sixth diode DD2 disposed between said output terminal IP3 and a connecting terminal P10, and a sixth inductance element LD2 disposed between said connecting terminal P10 and the ground; and

the transmitting circuit TX1 of said first transmitting/receiving system being connected to said input/output terminal IP1 by turning on said first diode DG1, said second diode DG2, said fifth diode DD1 and said sixth diode DD2.

3. The high-frequency switching module according to claim 2, wherein the impedance of said antenna terminal near a frequency band of the receiving circuit RX3 is adjusted by changing the constant of said sixth inductance element LD2, and the impedance of the receiving circuit RX3 of said third transmitting/receiving system.

4. The high-frequency switching module according to claim 2 or 3, wherein said diplexer is constituted by an LC circuit; wherein said first and second switching circuits are constituted by switching elements; wherein each transmitting part of said switching circuits comprises a lowpass filter constituted by an LC circuit; wherein at least part of the LC circuit of said diplexer, the LC circuit of said lowpass filter and inductance elements of said switching circuits are constituted by electrode patterns formed on dielectric layers forming a laminate; and wherein chip elements constituting part of said switching elements and said LC circuits are mounted onto said laminate.

5. The high-frequency switching module according to claim 4, wherein it further comprises a high-frequency amplifier integrally formed in said

laminate; said high-frequency amplifier comprising at least a semiconductor element, a voltage-supplying circuit and a matching circuit; at least part of inductance elements constituting said voltage-supplying circuit and said matching circuit and LC circuits being constituted by electrode patterns formed on said dielectric layers; and chip elements constituting part of said semiconductor elements and said LC circuits being mounted onto said laminate.